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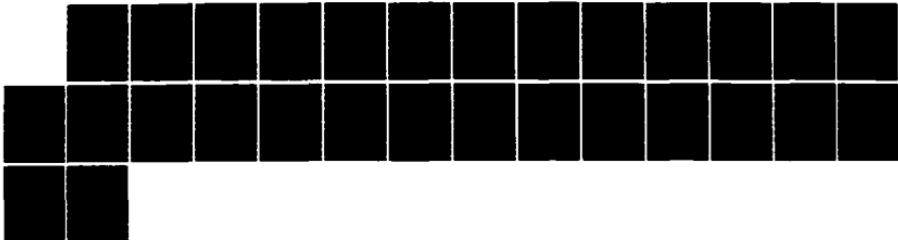
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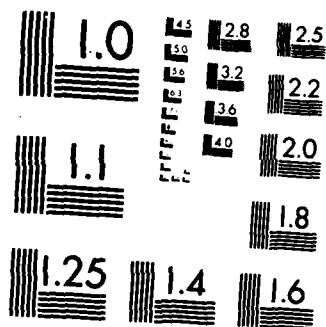
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## NONLINEAR REAL-TIME OPTICAL SIGNAL PROCESSING

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## 1.0 Summary

During the period 1 July 1984 - 30 June 1985, the research under Grant AFOSR-84-0181 has concentrated on four major areas. First, work has continued on an experimental sequential optical binary parallel architecture that is constructed from an array of binary optical switching elements (NOR gates) with interconnections done by a computer-generated hologram. We are examining new binary array SLM's, high efficiency, high space-bandwidth product (SBWP) interconnection holograms, and compact reflection versions of the general architecture with the intent of building a larger demonstration system with greater capabilities. Next, we have studied improved methods of providing the interconnections in these systems by the use of hybrid digital/analog (*facet*) holograms. We have examined analytical techniques for mapping circuit diagrams into gate locations and hologram arrays, and optimization procedures to determine the minimum set of necessary space-invariant basis functions and minimum set of space-variant indexing holograms. Another area of study has been the evaluation of devices and materials for high speed optical switching and bistability. Switching energies of 1 to 10 pJ and response times of 10 ns have been experimentally demonstrated at the University of Arizona for devices consisting of an array of Fabry-Perot cavities filled with a nonlinear material. We have begun to use the specifications of these devices and other high speed switching technologies in order to determine better designs and fundamental limits of the binary optical computing architectures under consideration. A final area of study has been to examine in detail algorithms that are well-suited for implementation on the parallel binary architectures described previously. We have defined several methods for building binary and arithmetic cellular logic processors and have determined some limits due to hologram complexity, gate density, etc.

## 2.0 Research Progress

This section summarizes research progress and accomplishments for the period 1 July 1984 - 30 June 1985 on Grant AFOSR-84-0181 for Nonlinear Real-Time Optical Signal Processing. These results are discussed separately in the sections that follow.

### 2.1 Digital Optical Parallel Computing Systems

We have continued studies on the applications of optics for parallel digital computing. This has included evaluation of optical logic devices (gates), arrays of devices (chips) and techniques for wiring or interconnecting the components to make an integrated processor.

Work on optical systems capable of implementing sequential binary digital logic operations has continued. The system consists of a spatial light modulator (SLM) used to provide a spatial array of photosensitive elements having a nonlinear threshold response, and a computer-generated hologram to provide interconnections among the photosensitive elements [JENK 84a], [JENK 84b]. Figure 2.1-1 shows a schematic diagram of the system.

In the present system the nonlinear element is a Hughes liquid crystal light valve (LCLV). We have implemented all the logic operations AND, NAND, OR, NOR, XOR, and XNOR optically using a parallel-aligned LCLV. Achieving these logic functions relies on an optical gate array having an intensity threshold input-output characteristic curve. Representing a logical 1 by a high intensity and a logical 0 by a low intensity, and superimposing the individual inputs to a gate onto pixels of the LCLV, device input levels of 0, 1, or 2 are possible for 2-input gates. Biasing and scaling the LCLV characteristic curve with available system parameters selects the logic operation being performed. For

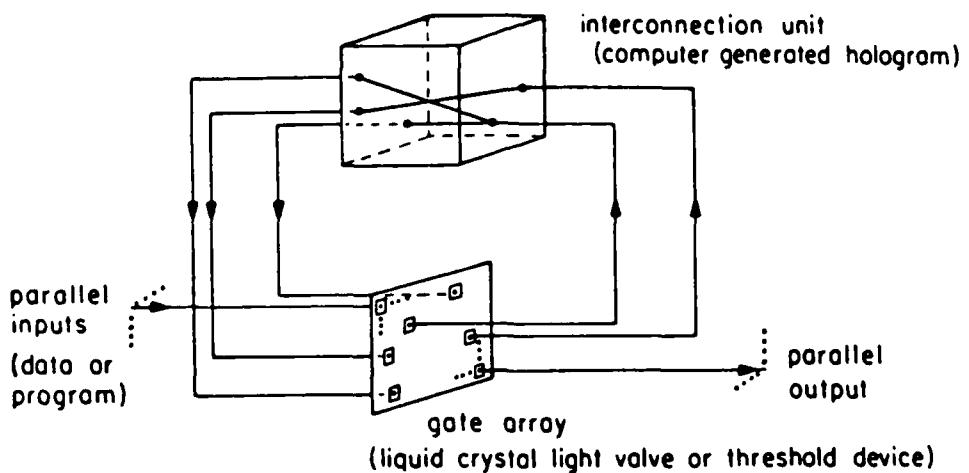


Fig. 2.1-1. Block diagram of the optical sequential logic system.

the logic gates in the sequential logic system we have used a  $45^\circ$  twisted-nematic LCLV. In general, it provides a monotonic input-output response and can be set up to implement the NOR operation if used in a negative slope mode. This is sufficient because the NOR operation is logically complete, i.e., all other Boolean operations can be built out of NOR gates.

The other major component of the sequential logic system is the interconnection network. Because these interconnections carry optical signals, we expect that they will be more immune to the interference and cross-talk problems frequently encountered in electronic systems. In our system a Lee-type computer-generated hologram (CGH) is used for the interconnections [LEE 70]. It consists of an array of subholograms, one for each gate output. The gate output array at the LCLV output is imaged onto the CGH. The Fourier transform is then taken via a lens to yield the hologram reconstruction

array at the LCLV input (Fig. 2.1-2).

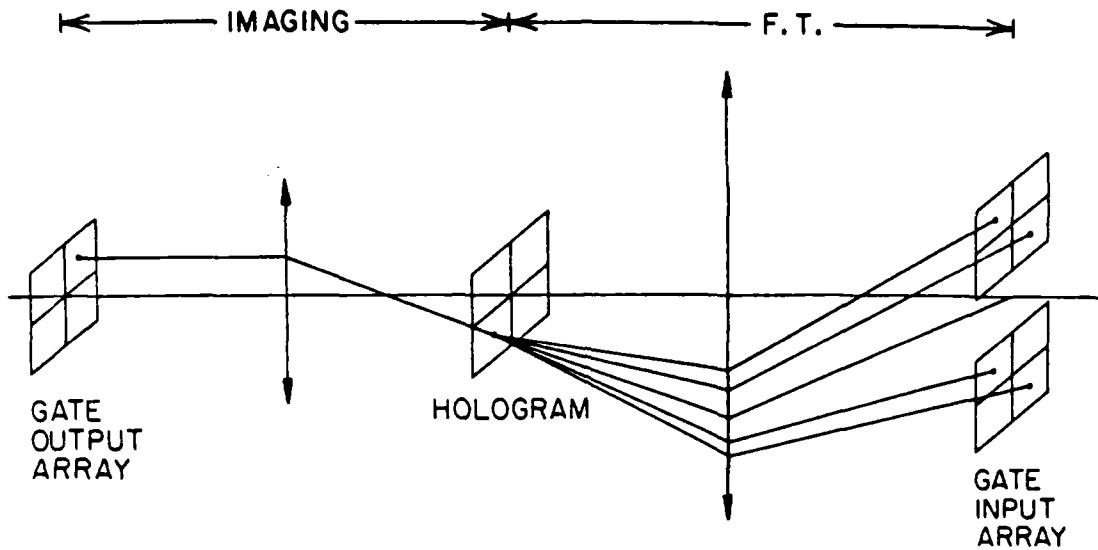


Fig. 2.1-2. Interconnection system using a space-variant hologram. The +1 reconstruction order is used for the LCLV input and the -1 order is used for probing.

Each subhologram reconstructs a pattern of points corresponding to the gate input connections. The CGH is analogous to the wires of printed circuit board of an electrical circuit, thus the particular circuit being implemented may be changed by swapping holograms in the optical system.

The system has been experimentally demonstrated using a twisted-nematic liquid crystal light valve as the SLM. A test circuit with 16 gates that includes a synchronous master-slave flip-flop and an oscillator consisting of five inverters in a feedback loop has been implemented. The circuit is shown in Fig. 2.1-3. To our knowledge, the system is the first that combines an all-optical sequential logic circuit with a self-contained clock.

Some of the interesting architectural features of the USC sequential optical proces-

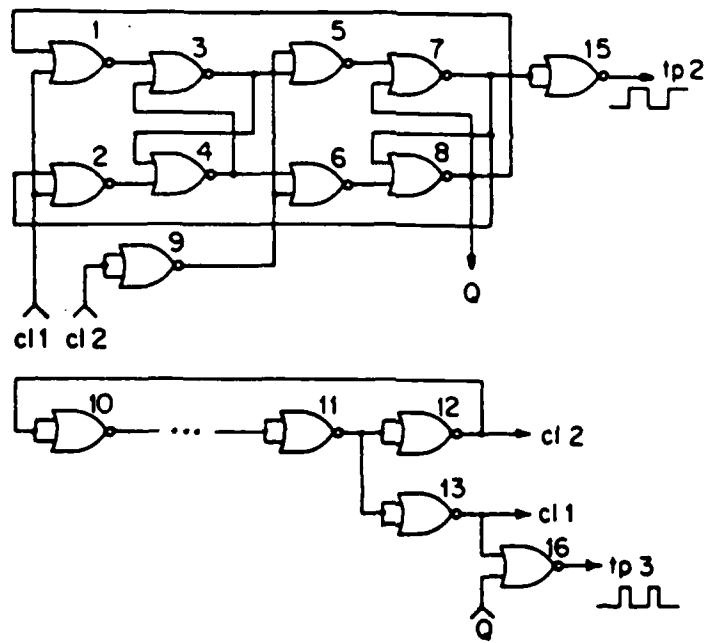


Fig. 2.1-3. Test circuit consisting of a synchronous master-slave flip-flop and a clock.

sor are:

- parallel input/output is possible - the pin-in and pin-out constraint problems of VLSI are not present
- the memory elements are integral with the processor gate array; all memory elements are made of flip-flops and no bistable elements are needed
- there is reduced differential signal propagation delay as compared to VLSI. All signal paths between gates are equal to first order. Arbitrary interconnections, both global and local, may be implemented with equal ease
- the system is software programmable and contains registers, instruction decoders, etc. that may be designed using tools similar to that for VLSI binary logic design.

- the interconnection hologram is the only major critical beamsteering component. It is made off-line under controlled conditions, and requires no multiple mirrors, prisms, or other beamsteering elements which may lead to alignment and stability problems

### **Compact System Implementation**

We are exploring some ideas for taking the existing architectural structure of the USC sequential digital optical processor and rearranging it into a more compact form. The present experimental system is much larger than necessary because it consists of an external feedback path placed around a Hughes liquid crystal light valve (LCLV). The feedback path goes through a beam-splitting and beam-directing hologram to provide the wiring on the LCLV gate array. We are considering the use of *reflective* beamsteering components (computer holograms, etc.) combined with a reflective logic gate array and appropriate prisms, polarizers and other optical components in order to make a compact processor. Such a system could have significant practical advantages in speed, power consumption, size, ease of alignment, stability, and ease of expansion (cascading of multiple processors).

Many experimental details on the optimization and adjustment of LCLV response, the computer-generated hologram used for interconnections, and the modeling and measurement of temporal response are summarized in two recent papers.

### **2.2 Interconnection Systems for Optical Computers**

We have continued work on extending the capabilities of optical sequential logic by carefully examining methods of interconnecting a 2-D array of optical gates with

computer-generated holograms (CGHs). Existing methods are: a space-variant (SV) technique (such as that shown in Fig. 2.1-2) which allows extremely general, arbitrary wiring, but is limited by the space-bandwidth product (SBWP) of the CGH; a space-invariant (SI) system which requires only very simple CGHs but suffers from low utilization of the gates available; and a hybrid space-variant/space-invariant technique that should provide large gate counts with high gate utilization. With the hybrid system, a space-variant element maps each gate through one of a library of fixed (or basis-set) space-invariant interconnection patterns. The goal is to implement an arbitrary circuit with a small number of interconnection patterns. Figure 2.2-1 shows the maximum number of gates possible assuming that the interconnection holograms have  $10^{10}$  resolution elements, a figure consistent with the use of existing e-beam lithographic systems, techniques and materials.

Fundamental Interconnection Method	Number of Gates	Number of Fundamental Interconnection Patterns	Required SBWP	Maximum No. of Gates
Space-variant (SV)	$N^2$	$N^2$	$\alpha N^4$	$10^4$
Space-invariant (SI)	$N^2$	1	$\alpha N^2$	$10^8$
Hybrid-two holograms (SV + SI)	$N^2$	M	$\alpha MN^2$	$10^7$ (with M=40)

$$(\text{No. of Gates}) (\text{No. of Int. Patterns}) = 4 \cdot 10^8$$

Holograms have  $10^{10}$  resolution elements - only local position accuracy needed

Fig. 2.2-1. Maximum number of gates for sequential optical logic system.

For the hybrid interconnection scheme that provides a reasonable compromise between a large number of gates and flexibility of interconnections, a maximum of  $10^7$  gates is predicted.

A significant problem with the hybrid approach is to simultaneously determine: the optimum labeling of gates corresponding to a circuit diagram; the corresponding minimum set of necessary space-invariant basis functions and minimum set of space-variant indexing holograms; the minimum necessary space-bandwidth product of space-invariant and space-invariant holograms. We refer to this problem as the *hologram compiler* problem because it is similar to the gate layout problem of conventional electronic VLSI. We are in the process of mathematically defining this process as an optimization problem, and we are exploring several types of numerical solution techniques. Existing results and software from VLSI design may be valuable in this effort.

We have been working on the use of volume hybrid analog/digital holograms (*facet holograms*) and general extensions of this concept as high efficiency (> 90%), high space-bandwidth product elements for gate interconnection in an experimental sequential logic system. Facet holograms are produced in dichromated gelatin by a computer-controlled step and repeat system. We are currently involved in evaluating specifications and design issues of these holograms for an experimental system.

### **2.3 Evaluation of Switching and Bistable Devices**

The most promising technology for gates has come from the area of optical bistability. Typically a nonlinear optical material is placed in a resonant (Fabry-Perot) cavity. The result is a nonlinear optical switch that can optionally provide a bistable response. For gates in an optical computer, a bistable response is not needed (or wanted). We

would like a logically complete set of operations to be possible. This requires either an inverting response, e.g. NOR, or AND and NOT, etc., or an inversion only at the input of the processor if both the signals and their complements are kept at every stage of the processor. For these reasons, an inverting response is preferred. Fortunately, these bistable devices can exhibit an inverting response.

## Devices

In the last few years rapid progress has been made in optical bistability for logic gates. Switching energies between 1 and 10 pJ have been experimentally demonstrated for devices that have response times of 1 to 10 ns [JEWE 84a], [JEWE 84b] and that have a NOR response (other responses have also been demonstrated.) These are non-linear materials in a Fabry-Perot etalon, and actually respond to power density, not total power. These devices typically switch much faster in one direction than the other, i.e. switch-on vs. switch-off (they are driven in one direction but relax in the other). The numbers quoted above refer to the slower of the two switching times.

Another promising device is the self electro-optic effect device (SEED) [MILL 85]. It is based on the effect of increasing absorption with increasing incident intensity. It utilizes electronics (voltage source and resistor) in addition to the optics. It has also been experimentally demonstrated, and has the lowest projected power of any usable device so far. The experimental device has  $600 \mu\text{m}$  diameter active area for one gate, and has an optical switching energy of  $\sim 1 \text{ nJ}$ ; this is an energy density of  $4 \text{ fJ}/\mu\text{m}^2$ . As the device is scaled down, its speed increases and its power requirements decrease. Scaled down to the physical limit ( $\lambda^2/n^2$  gate area), it has a projected power requirement of  $\sim 1 \text{ fJ}$  (electrical plus optical power). The importance of the power requirement will be

discussed below. Switch-off times of 400 ns were demonstrated (limited only by power), whereas switch-on were up to 5 times higher. Switching times of 1-10 ns look feasible.

Some pertinent results have been announced very recently. Partially successful results were reported of  $2 \times 4$  arrays of the Fabry-Perot etalon devices mentioned above for implementing NOR gates [JEWE 85] with spot (gate) diameters of 6-8  $\mu\text{m}$  and spacings of 30  $\mu\text{m}$ . The device was not completely uniformly thick, however, and the same gate operation was not achieved over all pixels (gates) simultaneously. In addition, a different device was reported [SHAR 85] that has demonstrated optical switching energies of 0.5-3.0 fJ and response times on the order of ns. This is a hybrid device and had total (electrical + optical) switching energy of approximately 20 pJ. It is an active device which is an InGaAsP laser amplifier in a resonant cavity. Arrays of large numbers of these may be more difficult to make due to power dissipation but in principle can be done. It also demonstrates that optical switching can be performed at these very low incident power levels, and is compatible with laser diode wavelengths. One other result was a 200 ps recovery time of optical gates in a Fabry-Perot etalon array [LEE 85]. This is the fastest recovery to date of an optical gate of this kind and is inherently suited to gate arrays. It was also performed in a GaAs/GaAlAs structure in a Fabry-Perot etalon.

Power is an important consideration, not only because of power dissipation of the elements, which puts constraints on how closely gates can be packed together, but because of the source power required. Statistically, 1000 photons per switching event are required for reliable switching [SMIT 82]. (This assumes the gate bases its decision on all 1000 photons, i.e. they all interact with the material. As some detectors have quantum efficiencies  $\sim 1.0$ , this may be achievable. Also, it is conceivable that there may be

ways of reducing this 1000 photon limit, but as yet there has not been any work in this area. This might be done by using other methods of encoding 1's and 0's, instead of intensity.) Devices that utilize a signal level encoded as intensity, as do the above bistable devices, are limited by this number. 1000 photons at  $\lambda = 0.5\mu\text{m}$  have an energy of 0.4 fJ. For an array of  $10^6$  gates switching every 1 nS, and allowing a factor of 5 for fan-out and other intensity losses, 2 W of optical power are required. This is approximately what today's highest power 1-D laser diode arrays can provide. The SEED device above, with a gate area of  $10\mu\text{m}^2$  (approximately the minimum that could be used in a gate array in an optical system) would require  $10^4$  to  $10^5$  photons per switching event. This is surprisingly close considering current spatial light modulators require  $\sim 10^9$  or more photons. Improvements in switching powers have been fairly rapid, and may continue to improve even more. An example is the switching laser amplifier device mentioned above with fJ switching energies.

### Materials

The most promising materials for bistable gates are III-V materials, particularly GaAs or GaAs/GaAlAs multiple quantum well (MQW) or superlattice structures (crystals that are essentially built by alternating thin layers of two materials to alter the microscopic and macroscopic properties), InSb, and InAs (the II-VI materials ZnSe and ZnS are also worthy of mention but are probably less promising), although there are other materials that may prove viable as well. The methods of molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) are important and extremely helpful in materials development. They essentially enable new (previously nonexistent) materials to be manufactured. The GaAs/GaAlAs MQW can provide sub-

stantially larger optical interaction coefficients than GaAs. The GaAs or GaAs/GaAlAs materials also have the advantage that they can easily be used at laser diode wavelengths (0.8-0.9  $\mu\text{m}$  is common).

#### 2.4 Algorithms and Architectures for Digital Optical Computing

We have been examining algorithms that are well suited for mapping onto parallel digital optical processing (DOP) architectures, including cellular logic processors (CLPs) [PRES 83], [DANI 81], [ROSE 83]. With the development of large optical gate arrays and methods of optically interconnecting them, there is the possibility of implementing parallel algorithms that may be impractical in VLSI. Image processing and image analysis tasks have large 2D data processing requirements and inherent parallelism, thus they are well suited to implementation in DOPs. Many pipeline, SIMD (single instruction-multiple data) and MIMD (multiple instruction-multiple data) architectures for such systems have been described [REEV 84]. Of particular interest are cellular logic processors (CLPs) which ideally place a digital arithmetic processor behind every pixel (cell) of an image with appropriate communications to other processors. The general architecture of CLPs has been studied since the early 1950s and several electronic hardware implementations have been constructed in the last 20 years. Many of these processors are highly specialized for applications in medical image processing, pattern recognition, x-ray analysis, and blood cell counting/discrimination. Most of these electronic CLPs directly communicate only in a local neighborhood around each pixel. In these systems, digital operations transform an array of data  $p(i,j)$  into a new array  $p'(i,j)$  in which the value of each element in the new array is determined only by its corresponding element  $p(i,j)$  in the original array along with the value of its nearest

neighbors. In general, extending the communications among individual cellular processors to longer distances greatly increases the speed and flexibility of tasks such as counting and hierarchical image processing/image analysis. CLPs can perform both binary pixel operations (which are adequate for many tasks) or gray-level operations (here the CLP can be thought of as a stack of 2-dimensional bit-slice processors). CLP's are well-suited to 2-D rectangular grid and repetitive processing operations that are natural for images. CLP's can perform binary operations or arithmetic operations on gray-scale images.

Many useful CLP operations can be directly performed on binary images by implementing a single operation or a repeated sequence of fundamental operations in the basic CLP instruction set. Some of these operations are:

- a.) pixel-by-pixel Boolean combinatorial logic functions
- b.) parallel recognition (cross-correlation, matched filtering or content-addressable memory) and replacement (symbolic substitution)
- c.) marking of boundary pixels of a region (edge detection or contour extraction)
- d.) morphological operations such as shrinking, expanding, convex hull extraction, exoskeleton extraction, thinning, filling, and endoskeleton extraction.

Gray-level operations on data with 8 or more bits per pixel are valuable for local enhancement (such as median filtering, small window convolution or smoothing), edge detection and linking, texture feature extraction, frame-to-frame comparison and differencing, gathering of image statistics and histogram measurements. Many other types of operations are used for data I/O and internal manipulation. These include:

- a.) testing values
- b.) scrolling of data in one of 8 directions
- c.) scanning pixels in raster format.

### Sequential Optical System Implementation of Cellular Logic

Figure 2.4-1 shows how one cell (one processor) of a cellular logic system could be implemented on the sequential optical processor system shown in Fig. 2.1-1.

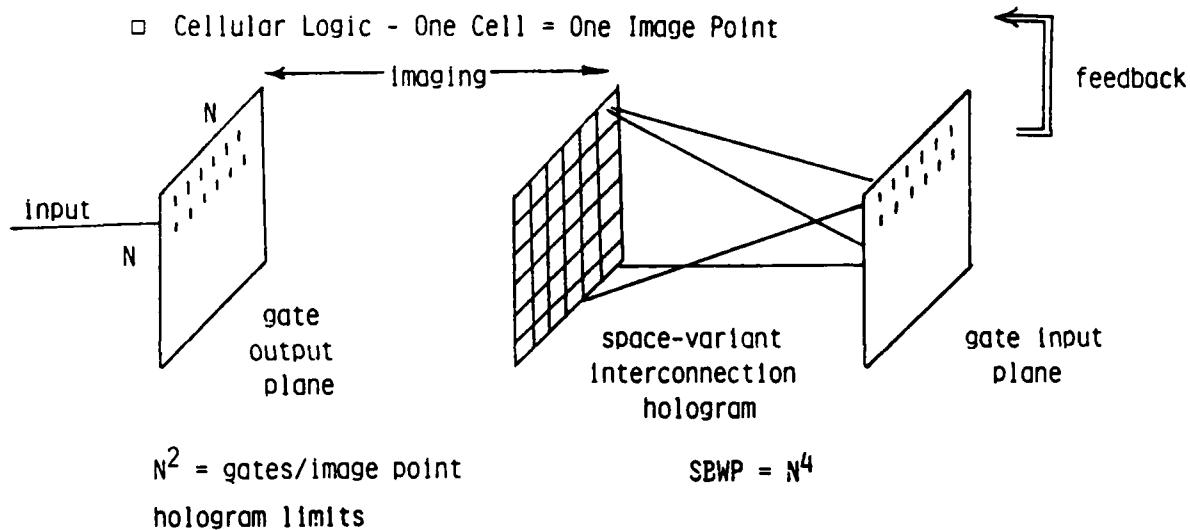


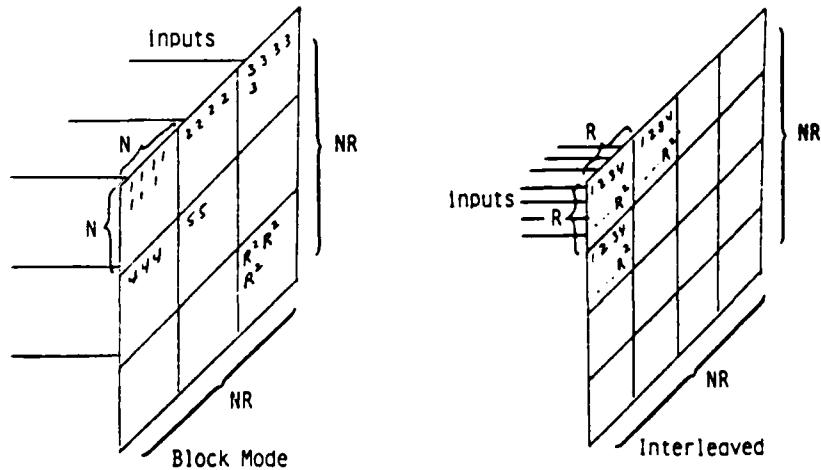
Fig. 2.4-1. One cellular logic cell (one processor) implemented using the optical sequential logic system of Fig. 2.1-1.

The optical input (a single image point) is directly detected by a sensor which transfers data (either binary or gray-level) to the gate array shown. There are  $N^2$  gates per image point (each is marked by a number 1 on the gate output plane shown). An image of the gate output array is transferred to the space-variant interconnection hologram, which directs the output beam(s) from each gate to the gate input plane shown at the far right

of the figure. An optical feedback system effectively connects the gate input plane to the left (front) side of the gate array, so that the hologram provides the wiring among the gates. The hologram thus requires a space-bandwidth product (SBWP) of  $N^4$ .

From recent work, we estimate that a low efficiency, e-beam thin binary phase hologram such as that used in the system of Section 2.1 could provide  $N^2 \approx 10^4$ . A high efficiency thick facet hologram (optically written under computer control) could provide  $N^2 \approx 2.5 \times 10^5$ . An optical copy of a thin hologram could potentially provide a sufficient SBWP so that  $N^2$  could be even larger. Section 3.2 discusses this in more detail.

The array of individual cellular logic processors for each image point now must be replicated to provide the complete array. We have examined two different techniques for this, called *block mode* and *interleaved mode*. These are shown in Fig. 2.4-2.



$N^2$  = gates per image point

$R^2$  = image points per chip

$N^2R^2$  = gates per chip

Fig. 2.4-2. Cellular logic replication techniques.

This figure shows the complete gate array for the whole processor, having  $N^2$  gates per image point,  $R^2$  image points per chip, and  $N^2R^2$  total gates per chip. In the block mode of operation, the gates associated with each input point (each processor) are given the same number (e.g. 1, 2, 3, etc., as shown) and are physically located nearby on the chip. In the interleaved mode, the  $R^2$  gates having the same exact function for all the  $N^2$  processors are physically located together, and the signal inputs for the entire system enter together as shown. In either case there are  $N^2R^2$  total gates per chip. Figures 2.4-3 and 2.4-4 show interconnection methods for these gates.

□ Cellular Logic - Block Mode

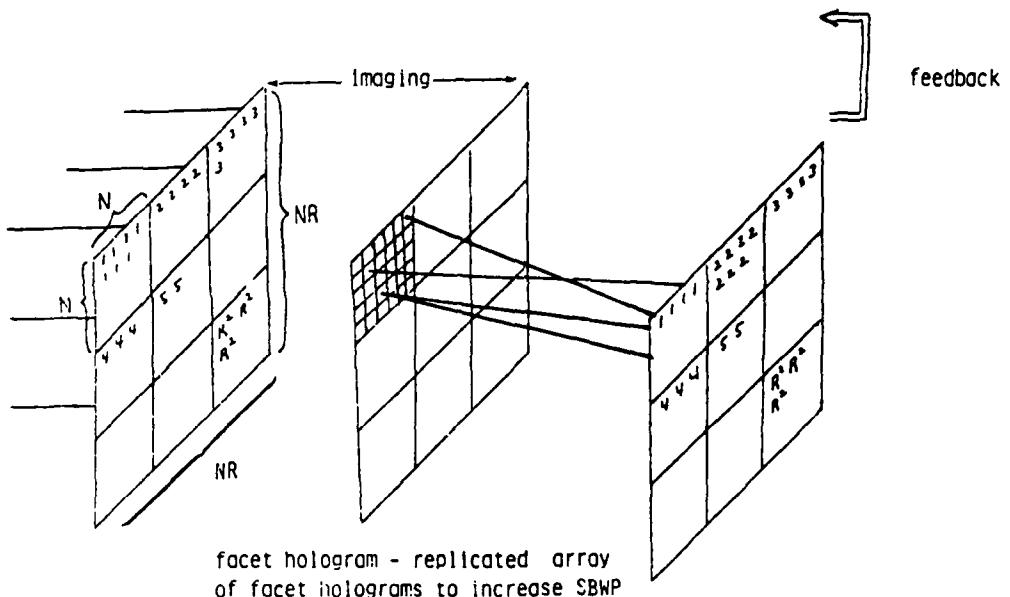


Fig. 2.4-3. Block mode cellular logic interconnection.

The block mode interconnection uses a replicated array of facet holograms to increase the SBWP up to the value of  $N^4R^2$  required. Here each image point processor is interconnected in an identical way, so the hologram is an array of identical replicated subholograms. The interleaved mode interconnection uses a different facet hologram array.

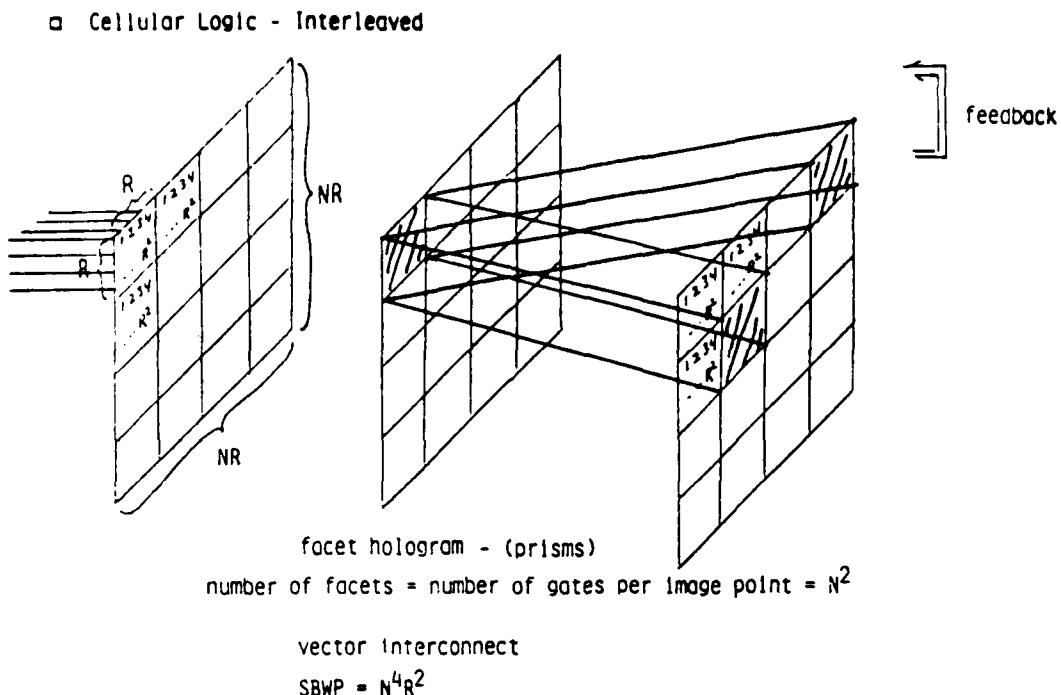


Fig. 2.4-4. Interleaved mode cellular logic interconnection.

Here the number of facets is equal to  $N^2$ , the number of gates per image point. Each facet hologram can be thought of as a complex prism which provides a *vector interconnection* of gates which are the same circuit element in each processor. The total required SBWP of  $N^4R^2$  is the same as for the block mode.

Figures 2.4-5 through 2.4-6 summarize the number of gates per chip and SBWP required to implement binary and arithmetic CLP's of various sizes.

In other recent work, we have been examining the capabilities of parallel DOP systems as a function of the various optical gate and interconnection technologies available now and projected in the future. The goal is to estimate the throughput, processing speed, number of processing cycles required for various operations and flexibility of these systems for a given set of assumptions. We have also begun to look at optical implementation of new 2-D cellular architectures having a denser set of inter-processor

□ Gates in a Cellular Processor - Binary

$R^2$ image points/chip	$N^2$ gates/ image point	$N^2R^2$ gates/ chip	$\frac{SBWP}{N^4R^2}$
512 x 512	32	$8.4 \cdot 10^6$	$2.7 \cdot 10^8$
512 x 512	256	$6.7 \cdot 10^7$	$1.7 \cdot 10^{10}$
256 x 256	32	$2.1 \cdot 10^6$	$6.7 \cdot 10^8$
256 x 256	256	$1.7 \cdot 10^7$	$4.4 \cdot 10^9$
128 x 128	256	$4.2 \cdot 10^6$	$1.1 \cdot 10^9$

Fig. 2.4-5. Gates in a binary cellular logic processor.

□ Gates in a Cellular Processor - Arithmetic

$R^2$ image points/chip	$N^2$ gates/ image point	$N^2R^2$ gates/ chip	$\frac{SBWP}{N^4R^2}$
512 x 512	2048	$5 \cdot 10^8$	$10^{12}$
512 x 512	1024	$2.5 \cdot 10^8$	$2.6 \cdot 10^{11}$
128 x 128	2048	$3.4 \cdot 10^7$	$7 \cdot 10^{10}$

Fig. 2.4-6. Gates in an arithmetic cellular logic processor.

communications than that available from planar VLSI. Some of these include the 2-D cellular hypercube and 2-D cellular pyramid.

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### 3.0 Written Publications

During the period 1 July 1984 through 30 June 1985, a number of papers have been published. A list of these follows:

1. A.A. Sawchuk, "Numerical Optical Computing Techniques", *Proc. 13th Congress of International Commission for Optics, ICO-13*, Sapporo, Japan, August 20-24, 1984.
2. A.A. Sawchuk and T.C. Strand, "Digital Optical Computing", *Proc. IEEE*, Vol. 72, pp. 758-779, 1984.
3. B.K. Jenkins, *et al*, "Sequential Optical Logic Implementation", *Applied Optics*, Vol. 23, pp. 3455-3464, 1984.
4. B.K. Jenkins, *et al*, "Architectural Implications of a Digital Optical Processor", *Applied Optics*, Vol. 23, pp. 3465-3474, 1984.
5. B.K. Jenkins and A.A. Sawchuk, "Characteristics of Digital Optical Processors", *Proc. IEEE Global Telecommunications Conf.*, Atlanta Ga., November 26-29, 1984.
6. B.K. Jenkins, "Architectural Characteristics of Optical Logic Systems", *Proc. IEEE Computer Conf.*, San Francisco, Ca., February 26-28, 1985.
7. B. K. Jenkins and A. A. Sawchuk, "Computer Generated Hologram Considerations for Sequential Optical Logic Interconnections", presented at Optical Society of America 1984 Annual Meeting, San Diego, October 29 - November 2, 1984.
8. A. A. Sawchuk and B. K. Jenkins, "Algorithms for Digital Optical Processors", *Tech. Digest for Topical Meeting on Optical Computing*, Optical Society of America, March 18-20, 1985, Incline Village, NV., pp. TuA2-1 - TuA2-4.

#### 4.0 Professional Personnel and Advanced Degrees

The following individuals contributed to the research effort supported by this grant:

Dr. Alexander A. Sawchuk, Professor of Electrical Engineering, Director, Signal and Image Processing Institute; Principal Investigator.

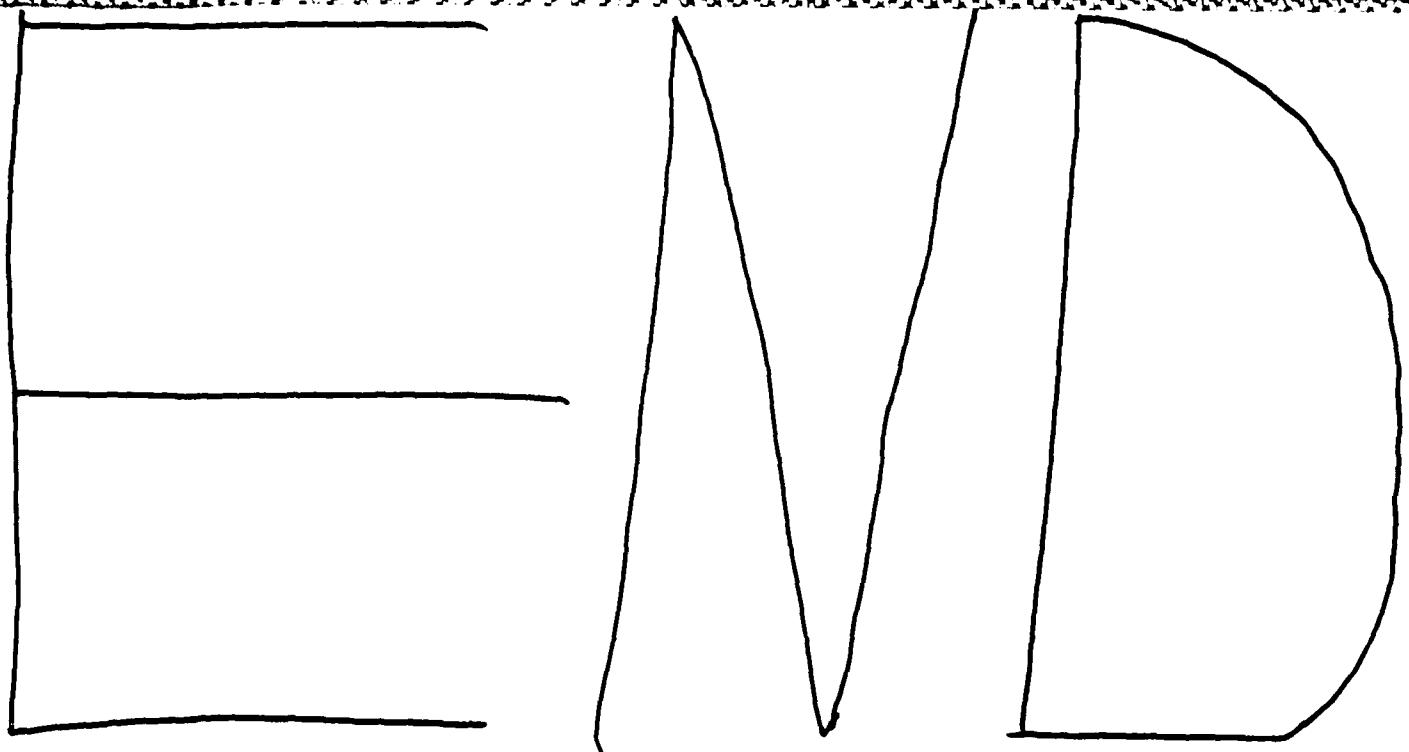
Dr. B.K. Jenkins, Research Assistant Professor of Electrical Engineering; Senior Investigator.

Herb Barad, Research Assistant, Ph.D. Candidate, Department of Electrical Engineering.

## 5.0 Interactions (Coupling Activities)

During the period 1 July 1984 through 30 June 1985, several oral presentations have been made at meetings and conferences based on this work. A list of these follows:

1. A.A. Sawchuk, "Numerical Optical Computing Techniques", *Proc. 18th Congress of International Commission for Optics, ICO-18*, Sapporo, Japan, August 20-24, 1984.
2. B.K. Jenkins and A.A. Sawchuk, "Characteristics of Digital Optical Processors", *Proc. IEEE Global Telecommunications Conf.*, Atlanta Ga., November 26-29, 1984.
3. B.K. Jenkins, "Architectural Characteristics of Optical Logic Systems", *Proc. IEEE Computer Conf.*, San Francisco, Ca., February 26-28, 1985.
4. B. K. Jenkins and A. A. Sawchuk, "Computer Generated Hologram Considerations for Sequential Optical Logic Interconnections", presented at Optical Society of America 1984 Annual Meeting, San Diego, October 29 - November 2, 1984.
5. A. A. Sawchuk and B. K. Jenkins, "Algorithms for Digital Optical Processors", *Tech. Digest for Topical Meeting on Optical Computing*, Optical Society of America, March 18-20, 1985, Incline Village, NV., pp. TuA2-1 - TuA2-4.



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